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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,086	08/17/2001	Georg Farkas	CH 000018	5457

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,086	FARKAS ET AL.	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4,5 and 10-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2, 4-5, 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *15 March 2004* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

GENERAL OFFICE ACTION

1. This office action is in response to Applicants' **Appeal Brief** of *07 December 2004*.

1.1 **Claims 2, 4-5, 10-13** remain pending.

1.2 The **finality of the last office action is withdrawn**. The period for Applicants to **reply shall therefore be restarted** as shown on Office Action Summary attached herewith.

1.2.1 The prior art rejections of record are withdrawn in response to Applicants' **Appeal Brief**.

Claim Rejections - 35 USC ' 102

2. **Claims 2, 4, 10-13 (is)** are rejected under 35 U.S.C. 102 (e) and (b) as being anticipated by Frey **et al.** (US Pat. # 6430720; FILED: June 23, 1998) (claim 12) and **Attaway et al.** (US Pat. # **5,872,793) (Claims 2, 4, 10-13)**.

As per claim 12,

Frey anticipates claim 12 because Fig. 1 along with col. 5 line 40 et seq. discloses a vector memory that generates test vectors and relaying such test vectors to IC for application of such test vectors by such IC to test embedded logic or combinational circuitry.

2.1 **Attaway et al.** anticipates **claims 2, 4, 10-13** because Figs. 1-6 depict 'on the fly ' or real time generation of test vectors via, e.g., pseudo-random/algorithmic means along with BIST or self-testing for testing logic circuitry of an IC with equivalent means to receive test vector from external tester, testing logic circuitry, receiving from logic circuitry test vector results, compressing or compacting said test vector results, result analyzing means and outputting said compressed or compact test vector results to said external tester.

Claim Rejections - 35 USC § 103

3.0 Claim(s) 5 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over **Attaway et al.** and Derwent Abstract ACC-NO 1988-141950 (hereinafter Dias).

Attaway et al., however, does not teach in detail of using a programmable test vector generator that includes an ALU (i.e. processor). **Dias** in an analogous art, teaches of using a processor to feed a test vector generator with the required characteristics of the system. The processor is used to determine the test vectors used, see page 2 of Dias under "Basic-Abstract."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement programmable test vector generator made up of ALU as in Dias. One of ordinary skill would have been motivated to do so by the suggestion of Dias that by using processor to help determine the test vectors used, a smaller number of vectors are required while being able to detect all faults (i.e. maintain coverage) in a circuit, see page 2 of Dias under "Equivalent-Abstract."

3.1 Claim(s) 10 and 4 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Frey et al. in view of **Barry et al.** (US Pat. # 5825785).

As per claim 10,

Frey et al. substantially teaches of testing integrated circuits using a test system that is included in the IC to be tested. Further, Frey et al. teaches of using test vector pattern generators to generate test vectors, and of using test vector pattern generators as an alternative to loading the test vectors into large test memories.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a test vector pattern generator as described by Frey et al. in Figure 1. One of ordinary skill in the art would be motivated to use a test vector pattern generator in the embodiment so as to prevent from having to use a large test memory as suggested by Frey et al. By replacing the large test memory with a test pattern generator, one of ordinary skill in the art would save IC space and cost by not having to implement the test vectors in large test memories.

However, Frey et al. does not teaches of exclusively generating test vectors for logic circuitry, but **Barry et al.** discloses a BIST arrangement wherein test vectors are created exclusively for logic circuitry testing in Fig. 1 and col. 8.

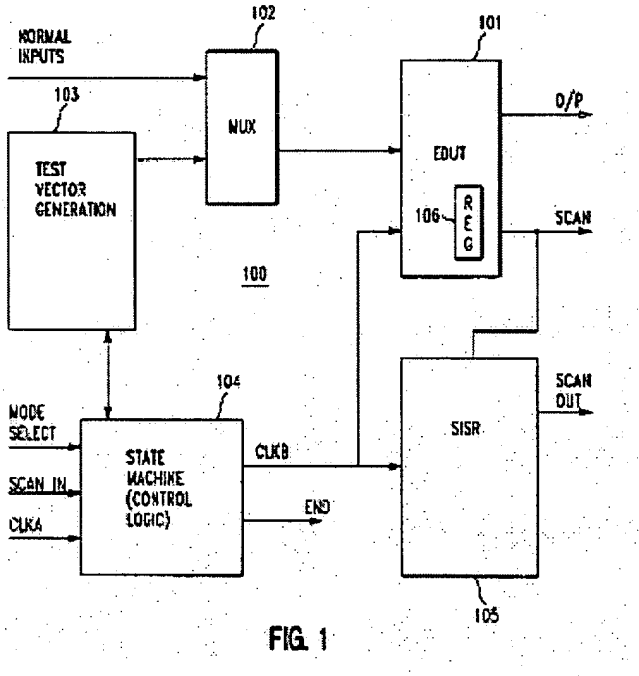

FIG. 1

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the **invention** was made to modify the procedure in Frey et al. by including therein BIST arrangement as taught by **Barry et al.,** because such modification would provide the procedure disclosed in Frey et al. with a technique whereby "*test vector application to inputs of said embedded macro circuit causes said embedded macro circuit to generate a response on the parallel outputs for (e) serially shifting said response from said scan register into a serial input shift register (SISR) such that each subsequent response is serially compressed with a previous response in said SISR resulting in a signature of said each response in said SISR.*" {See **Barry et al.,** col. 8 line 45 et seq.}.

Claim(s) 4 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Frey et al. in view of **Barry et al.** (US Pat. # 5825785) and Attaway et al. (US Pat. # **5,872,793**).

As per claim 4,

Frey et al. does not teach that compressing the response vectors into a single signature/checksum is effected. However, **Attaway et al.** does, e.g. in Abstract and Fig. 4: Mux 22(below).

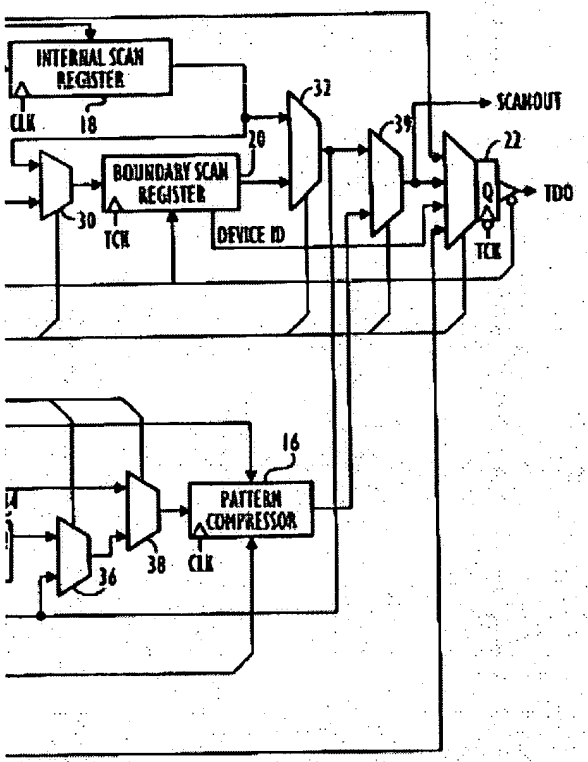

FIG.4

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the **invention** was made to modify the procedure in Frey/Barry al. by including therein vector compression as taught by **Attaway et al.,** because such modification would provide the procedure disclosed in Frey/Barry et al. with a technique whereby test *result storage requirements are optimized.*

3.2 Claim(s) 5 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Frey et al.) in view of **Barry et al.** (US Pat. # 5825785) and **Attaway et al.** in further view of Derwent Abstract ACC-NO 1988-141950 (hereinafter Dias).

As per claim 5,

Frey/ **Barry/Attaway et al.** substantially teaches, as combined above in claim 10, the limitations of claim 5.

Frey/ **Barry/Attaway et al.** however, does not teach of using a programmable test vector generator that includes an ALU (i.e. processor).

Dias in an analogous art, teaches of using a processor to feed a test vector generator with the required characteristics of the system. The processor is used to determine the test vectors used, see page 2 of Dias under "Basic-Abstract."

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the programmable test vector generator of Dias instead of the test vector generator of Frey/ **Barry/Attaway et al.** in the arrangement of Frey et al.. One of ordinary skill would have been motivated to do so by the suggestion of Dias that by using processor to help determine the test vectors used, a smaller number of vectors are required while being able to detect all faults (i.e. maintain coverage) in a circuit, see page 2 of Dias under "Equivalent-Abstract."

3.3 Claim(s) 11-13 and 2 is/are rejected under 35 U.S.C. 103(a) as being unpatentable over Frey et al. in view of **Barry et al.** (US Pat. # 5825785).

As per claims 11-12,

Frey et al. substantially teaches of testing integrated circuits using a test system (Figure 1) and a logic component/block that is included in the IC to be tested.

Further, Frey et al. teaches of using test vector pattern generators to generate test vectors. Still further, Frey et al. teaches that using test vector pattern generators is an alternative to loading the test vectors into large test memories.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a test vector pattern generator in an embodiment as described by Frey

et al. in Figure 1. One of ordinary skill in the art would be motivated to use a test vector pattern generator in the embodiment so as to prevent from having to use a large test memory as suggested by Frey et al. in lines 10-14 of page 1. By replacing the large test memory with a test pattern generator, one of ordinary skill in the art would save IC space and cost by not having to implement the test vectors in large test memories.

However, Frey et al. does not teaches of compressing test results from the logic circuitry, but **Barry et al.** discloses a BIST arrangement wherein such test result compression means is effected in Fig. 1:block 105 via *sisr*.

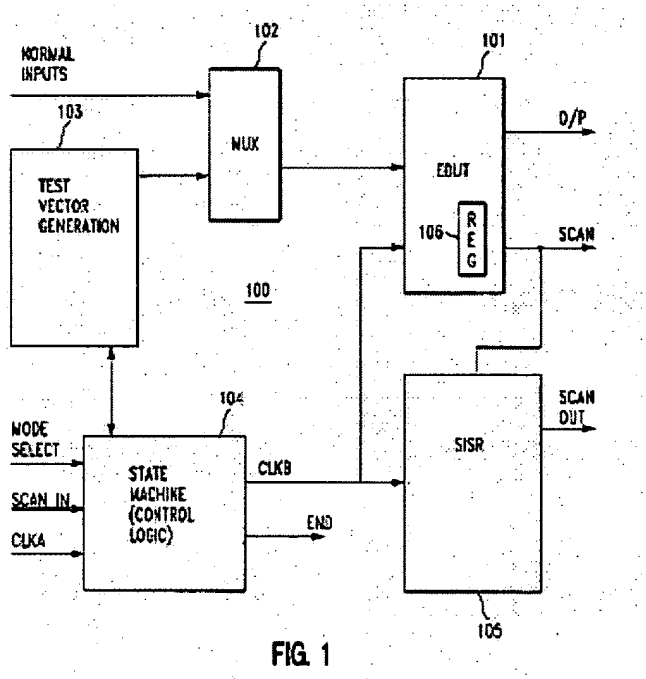

FIG. 1

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the **invention** was made to modify the procedure in Frey et al. by including therein BIST arrangement as taught by **Barry et al.,** because such modification would provide the procedure disclosed in Frey et al. with a technique whereby "*test vector application to inputs of said embedded macro circuit causes said embedded macro circuit to generate a response on the parallel outputs for (e) serially shifting said response from said scan register into a serial input*

shift register (SISR) such that each subsequent response is serially compressed with a previous response in said SISR resulting in a signature of said each response in said SISR. " {See **Barry et al.,** col. 8 line 45 et seq.}.

As per claim 2,

Frey et al. further teaches of an IC including a test analysis unit (5 of Figure 2) for compressing response vectors and a test control block (6 of Figure 1 and 2) for controlling the test procedure. Since both Figures 1 and 2 are known descriptions of the art, it would have been obvious to one of ordinary skill to combine the integrated test analysis unit of Figure 2 into the IC of Figure 1. Since both embodiments are known in the art, it would have been an obvious step to one of ordinary skill in the art to include the analysis unit. Further, one of ordinary skill would have known that by implementing a test analysis unit on chip, it would allow the system to only be required to send the signature (i.e. compressed responses) instead of all of the test response vectors. Because of the compression of the responses into a single signature, less data would have to be transferred (i.e. single signature vs. all of the response vectors) thereby increasing the speed at which an IC is tested. **Barry et al.** also teaches similar compression means via *a serial input shift register (SISR)* 105 in col. 8 lines 14 and 45 et seq.

As per claim 13

Barry et al. also teaches similar testing and compression means via *a serial input shift register (SISR)* 105 in col. 8 lines 14 and 45 et seq. for output to an output terminal.

Conclusion

. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Customer Services, 220 20th Street S., Crystal Plaza II, Lobby, Room 1B03, Arlington, VA 22202.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
May 2, 2005